Novel Digital Voltage Ramp Generator for Use in Precision Current Sources in the Picoampere Range

Gerd-Dietmar Willenberg and H. Norbert Tauscher

***Abstract*—We report on the development of a novel highly linear voltage ramp generator to be used for the traceable calibration of picoamperemeters. The generator is based on two digital-to-analog converters, one of them being used to compensate for the differential nonlinearity of the other one. The generator is completely controllable by a computer, its voltage slope dV/dt is adjustable between 1 and 1000 mV/s. During a ramp running between -10 and $+10$ V, the slope shows a relative variation of only $1.3 \cdot 10^{-5}$ (relative standard deviation). Due to a small output filter time constant of only 10 ms, we are, for the first time, able to conduct dynamic measurements of picoamperemeters with no sacrifice of linearity.**

***Index Terms*—Ammeters, calibration, current measurement, digital–analog conversion, signal generators.**

I. Introduction

In the current range below 1 nA, the most favorable way to obtain precise and traceable calibrations of amperemeters relies on charging a gas-filled capacitor of capacitance C by means of a linear voltage ramp of a constant slope dV/dt (see Fig. 1). The current thus generated $I = C \cdot dV/dt$ is used as the calibration current. By measuring the capacitance C and the slope dV/dt, the current is traced back to the SI units farad, volt, and second.

In this setup, the voltage ramp generator is a key component, since the current's stability crucially depends on the properties of the voltage ramp generator. Any nonlinearity of the slope produces a corresponding change in the current. Up to now, nearly all voltage ramp generators employed for precision measurements were based on electronic integrators. Unfortunately, these integrators suffer from the nonideal properties of their integration capacitors such as leakage and dielectric absorption [1], which lead to some nonlinearity of the voltage ramp. In the past, several works have been published that deal with this problem.

In [2], a sophisticated compensation network using analog electronics was developed which had been adjusted in an iterative procedure. Recently, a similar system has been set up by Kim *et al.* [3].

In contrast to this, van den Brom *et al.* [4] compensated for the integrator errors by adjusting the integrator's input current with the aid of a digital-to-analog converter (DAC), which was controlled by a computer that had "learned" the integrator's behavior during several test runs.

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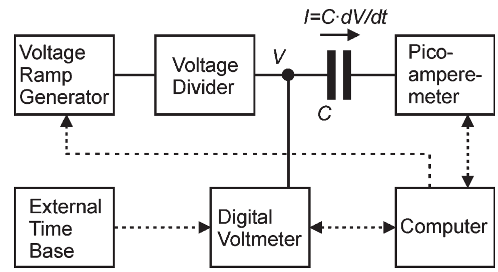

Fig. 1. Principle of calibrating a picoamperemeter using a voltage ramp generator and a gas-filled capacitor.

Likewise, Mortara *et al.* [5] used a DAC to inject a compensation current into the integrator's input. However, in contrast to [3], they omitted the learning runs. Instead, in their setup, the compensating current is determined during the running ramp by simultaneously measuring the voltage slope and calculating the appropriate compensation current.

A different approach was used by Callegaro *et al.* [6], who physically compensated only for the capacitor's leakage by using a feedback network, whereas the dielectric absorption was taken into account during the subsequent data processing.

In [7], Fletcher *et al.* completely circumvented the problem of dielectric absorption by using an air capacitor for the integration capacitor, but with this approach, the usable capacitance was limited to 10 nF.

Recently, two ramp generators have been presented that completely avoided analog integrators [8], [9]. Instead, the voltage ramp was generated directly by DACs, which were controlled by appropriate digital electronics. Whereas, in [8], a single DAC has been used, in [9], a pair of DACs has been used, and they have been arranged in such a way that one of the DACs improves the resolution and the differential nonlinearity of the other one. Due to its design, it allows rapid changes in the voltage slope and, therefore, also in conducting dynamic measurements. In this paper, the generator in [9] is presented in much more detail, and additional new measurements are shown.

II. Principle

Ramp generators based on DACs offer some favorable features: Their stability relies only on the stability of the DAC's voltage reference and on the stability of the clock frequency [9]. Furthermore, it is possible to change the slope dV/dt by a simple software command.

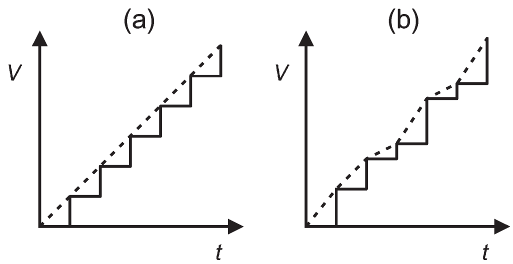

Fig. 2. (a) Example of the successive steps of an ideal DAC. All steps are of equal height. This pattern could, with some effort, be smoothed to form a highly linear voltage ramp (dashed line). (b) Successive steps of a real DAC. The step heights vary due to their differential nonlinearity. This pattern is very hard to smooth when forming a highly linear voltage ramp.

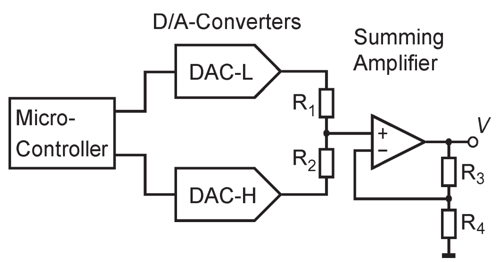

Fig. 3. Block schema of the digital ramp generator with two DACs. The DACs' output voltages are added using different weights.

However, ramp generators relying on one DAC suffer from the unavoidable differential nonlinearities of commercially available DACs and from their limited resolution. Due to the differential nonlinearity, the steps are not all equally high. Therefore, it is very difficult to smooth the steps to form a sufficiently linear voltage ramp, as depicted in Fig. 2.

This is particularly unfavorable in the case of slow ramps with low dV/dt, since in that case, there would be only very few steps per second and their variation in height would become particularly detrimental. Therefore, for smoothing such a ramp, a low-pass filter with a long time constant would be necessary, which would consequently lead to long settling times.

The key observation that allowed us to solve this problem was that for a given precision DAC, the heights of its steps may vary from one step to the other, but each individual step height is very reproducible over time. Therefore, it should be possible to take the different step heights into account using an appropriate algorithm.

Considering this knowledge, a novel ramp generator has been projected that makes use of two DACs controlled by one microcontroller, as shown in Fig. 3.

The output voltages of the two DACs are summed with different weights in such a way that at the summing amplifier's output, the steps of one DAC ["high DAC" (DAC-H)] are much higher than the steps of the other DAC ["low DAC" (DAC-L)]. This is done by adjusting the ratio $\mathrm{R}_1/\mathrm{R}_2$ to the desired ratio; in our case, it is 256 : 1. DAC-L is used to produce small voltage ramps that fit in between the steps of DAC-H, as depicted in Fig. 4. This requires the controller to "know" DAC-H's step heights in advance. For decreasing ramps, an equivalent algorithm is implemented.

It should be noted that it is characteristic for this procedure that DAC-H's steps are not equally long but that each step has rather its individual length, depending on its height (see Fig. 4).

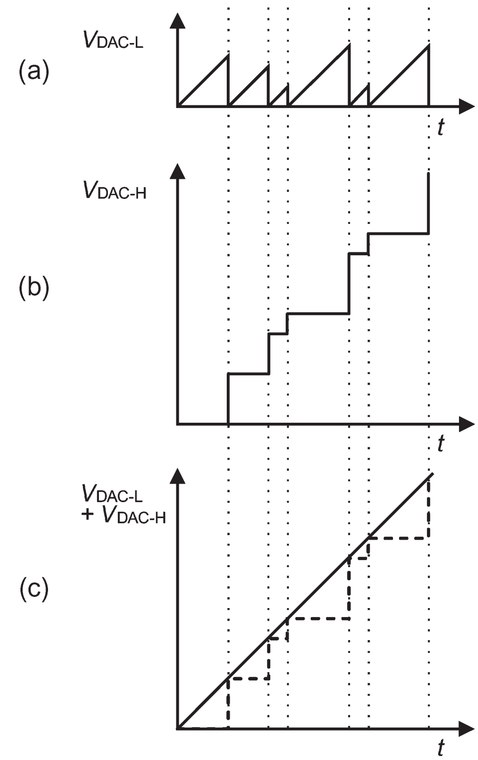

Fig. 4. Voltages at the summing amplifier's output. (a) Contribution of DAC-L. (b) Contribution of DAC-H. (c) Resulting voltage. The voltage steps of DAC-L are small enough to become unrecognizable in the scale chosen.

III. Realization

Up to now, two prototypes have been built, each with basically the same hardware: two 16-bit DACs (Linear Technology LTC1821) are controlled by a common microcontroller (Atmel ATmega128), operating at a clock frequency of 16 MHz. The outputs of DAC-H and DAC-L are added using a weighing ratio of 256 : 1, i.e., on the average, DAC-L runs from 0 to 255 until it is reset to zero, and DAC-H is incremented by one. This gives a virtual resolution of 24 bits. The clock frequency for the DACs is derived from the controller's clock using the controller's internal frequency divider.

The overall ramp slope is adjusted by choosing an appropriate DAC clock frequency. In the present software version, this frequency is limited to 45 kHz. If this frequency is not high enough to achieve a very fast ramp, then DAC-L's increment can be increased from one to any other desired value, which allows for a lower DAC clock frequency to be chosen. In general, it is preferable to use a DAC clock frequency as high as possible and a DAC-L's increment as low as possible. As the parameters may be freely combined, the ordinarily used voltage slope ranges between 1 mV/s and 1 V/s can be easily covered without any external components.

To take into account the different step sizes of DAC-H, each step was measured using an Agilent 3458A digital voltmeter (DVM). From these data, a table of correction values was calculated and stored permanently in the microcontroller's

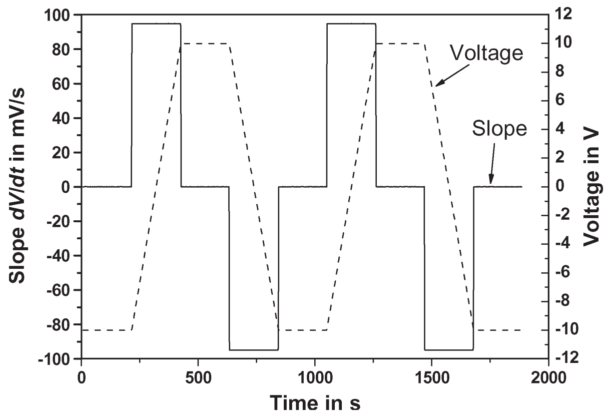

Fig. 5. Output voltage V of the ramp generator (dashed line), together with its slope dV/dt (solid line).

memory. The microcontroller uses these data to determine the lengths of the small ramps produced by DAC-L.

The ramp generator is completely controllable by text commands sent to its serial interface. There are no manual controls at the front panel; there is merely a liquid crystal display to show the current ramp status. For test purposes, the feature "variable step length" can be disabled by sending a special software command. In this state, DAC-L is always incremented to 255 until it is reset, and DAC-H is incremented.

In the present experimental versions, there is no internal low-pass filter in the signal path. Instead, we used an external passive first-order low-pass filter at the output. As the output signal contained only very short spikes of about 10-ns length, we found a time constant of 10 ms to be sufficient to avoid any disturbances of the measurement and of the picoamperemeters to be calibrated.

IV. RESULTS

To demonstrate the ramp generator's performance, the voltage profile shown in Fig. 5, which is typically used for calibrating picoamperemeters (see also [3] and [4]), has been generated and measured.

The profile consists of several cycles, each of which contains four phases: In the first phase, the voltage is resting at a negative voltage, producing zero current. In the second phase, the voltage increases linearly with time, producing a constant positive current. In the third phase, the voltage is resting at a positive voltage, producing zero current again. In the fourth phase, the voltage decreases linearly with time, producing a constant negative current. After a predetermined number of cycles, a finishing zero-current phase is added.

Whereas Fig. 5 gives an overview of the generated waveform, some parts are enlarged in Fig. 6(a)–(c) to show more details. All measurements of the voltage and the slope have been performed using a DVM of the Agilent 3458A type, triggered periodically by a precision time base, with a period of 0.9 s. The DVM's integration time was always set to 100 ms.

In Fig. 6(a), the voltage slope during the zero-current phases is shown. In these phases, the voltage generator is in a state where the DACs are neither incremented nor decremented, but they are being refreshed repeatedly with the DAC clock

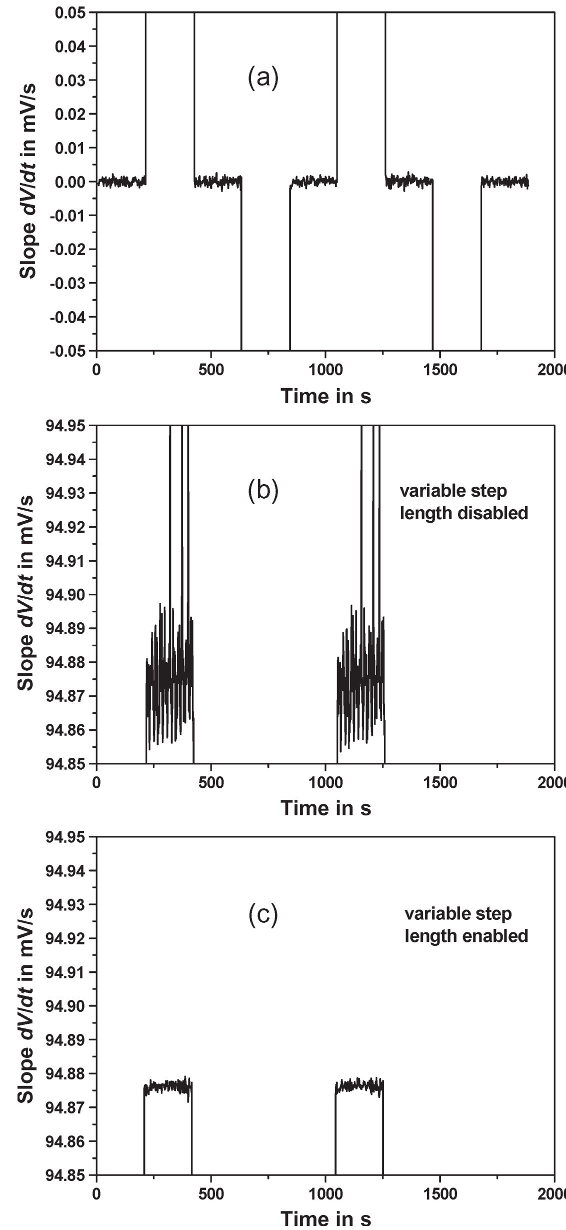

Fig. 6. Enlarged parts of the ramp generator's output voltage slope showing stability and noise, all using the same scale. (a) For zero-generated currents, the DACs are not incremented or decremented, but they are refreshed at the DAC's clock frequency with the same constant value. Therefore, some noise due to analog electronics and due to glitches is visible. (b) For positive generated currents, the feature "variable step length" was disabled. The noise is mainly due to the differential nonlinearity of DAC-H. (c) For positive generated currents, the feature "variable step length" was enabled. The noise is greatly reduced with respect to (b), but there is still some contribution of DAC-H's differential nonlinearity.

frequency to a constant digital value. Therefore, the still visible noise can be attributed to the noise of the analog electronics and to possible glitches from the digital part. No correlations between the noise patterns of different cycles have been found.

Fig. 6(b) shows the slope during the phases for positive current, while the feature "variable step length" had been disabled. The noise pattern has a periodic structure that reflects the internal structure of DAC-H. This is shown more clearly in [9, Fig. 2(a)]. The patterns of the subsequent cycles are highly correlated with a correlation coefficient very close to 1.0,

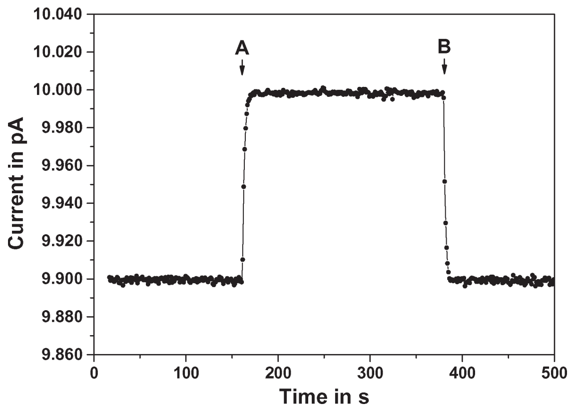

Fig. 7. Response of a commercial picoamperemeter (Keithley 6430) to sudden current changes. The current was generated using an air capacitor of 1000-pF capacitance (General Radio GR1404). At the beginning, the voltage slope was 9.9 mV/s, at point A, it was increased to 10.0 mV/s, and at point B, it was decreased to its initial value again. The picoamperemeter's settings were sample time = 200 ms and repeat-filter setting = 3. Its readings were recorded with a repetition rate of 1 s. An analysis of the values results in a time constant of 1.8 s for the picoamperemeter.

also indicating that the noise is mainly due to the differential nonlinearity of DAC-H. The relative standard deviation of the noise is $1.3 \cdot 10^{-3}$.

In Fig. 6(c), the slope is shown again during the phases for positive current, but in contrast to Fig. 6(b), the feature "variable step length" had been enabled. Now, the noise is reduced by a factor of 100 to a level slightly above that of the zero-current phases [see Fig. 6(a)], and no periodic structure is visible (see also [8, Fig. 2(b)]). The relative standard deviation is $1.3 \cdot 10^{-5}$, a value that matches nearly exactly the noise level of $1.2 \cdot 10^{-5}$ of our old voltage ramp generator constructed entirely in analog electronics [2]. The noise patterns of the different cycles are still correlated with a correlation coefficient of about 0.6, indicating that part of the noise is still due to the differential nonlinearity of DAC-H. Therefore, there is still some potential for future improvement.

For negative voltage slopes, the results are equivalent to those for positive slopes; therefore, they are not shown here.

As mentioned above, the device allows for the studying of the time behavior of picoamperemeters by applying sudden changes of the generated current. This is demonstrated in Fig. 7, where the slope is dV/dt, and with it, the generated current have been successively increased and decreased by 1%. The measured time constant of the picoamperemeter was 1.8 s. More details are given in the figure captions.

Some first calibrations of picoamperemeters have been performed using the new generator. The uncertainties obtained were about equal to those obtained with our analog voltage ramp generator [2]. This was as expected, as at the linearity level achieved, the major contribution to the uncertainty budget stems from the device under test and from other sources, e.g., from the capacitor or from the cables (see, e.g., [9]).

V. Conclusion and Outlook

A novel type of a highly linear digital voltage ramp generator has been developed that will replace our previously used integrator-based ramp generator in the setup for calibrating picoamperemeters. It makes use of two DACs controlled by a microcontroller by using a special algorithm.

In contrast to the old ramp generator, where different voltage slopes had to be manually adjusted using a voltage divider, the new system is much more versatile as it allows the choice of any desired voltage slope by simply issuing a software command, even during a running ramp. Thus, the normally used voltage slope range between -1 and 1 V/s can be easily covered without any external components.

Up to now, two prototypes have been constructed. Their noise properties are comparable with our previously used voltage ramp generator, based on an electronic integrator. Some first picoamperemeter calibrations have already been performed using the new generators. Although the new setup reduces the calibration uncertainties only to a small extent compared with the previously used analog ramp generator, it considerably simplifies the calibration procedure. Due to the very short time constant of its low-pass filter of only 10 ms, it will, for the first time, enable us to perform dynamic measurements of picoamperemeters.

Furthermore, another aspect has to be noted. As the generated voltage slope depends only on the clock frequency and on the DACs' reference voltage, the slope is intrinsically very stable. This stability could even be increased by applying a temperature stabilization. Therefore, in the future, it might be possible to omit the DVM in the calibration setup (see Fig. 1), which would significantly simplify the calibration setup. This approach would require periodical traceable recalibrations, as well as a study of the instrument's long-term stability and behavior with respect to ambient conditions. The latter work will be a task for the future.

We have applied for a patent for the technique used. It is planned to make the voltage ramp generator commercially available in cooperation with an external company.

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